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(54) **AMPLIFIER CIRCUIT**

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(57) **ABSTRACT**

An amplifier circuit comprises an input, for receiving an
input signal to be amplified; a preamplifier, for amplifying
the input signal based on a variable gain; a power amplifier
for amplifying the signal output from the preamplifier; and
a variable voltage power supply for supplying one or more
supply voltages to the power amplifier. The supply voltages
are adjusted based on the variable gain or the input digital
signal. According to other aspects of the invention, a power
supply of an amplifier circuit is clocked using a clock signal,
whereby the clock signal has a frequency that varies in
accordance with a volume signal or an input signal.

15 Claims, 15 Drawing Sheets
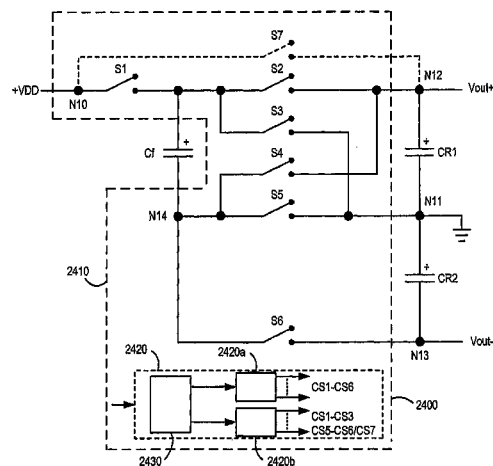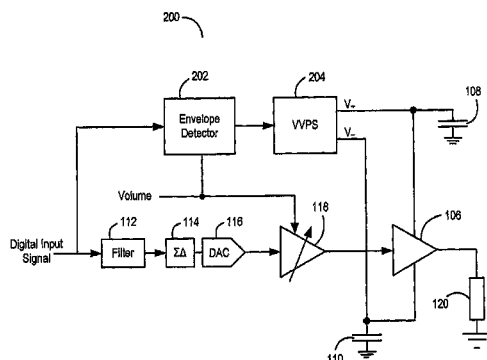
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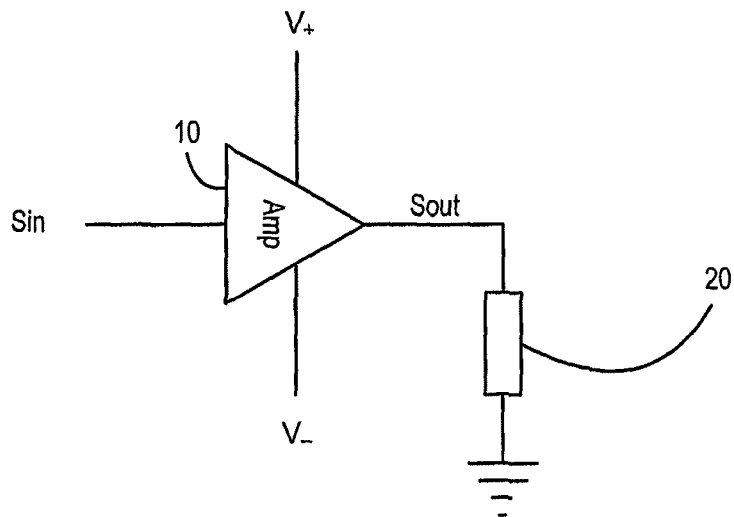
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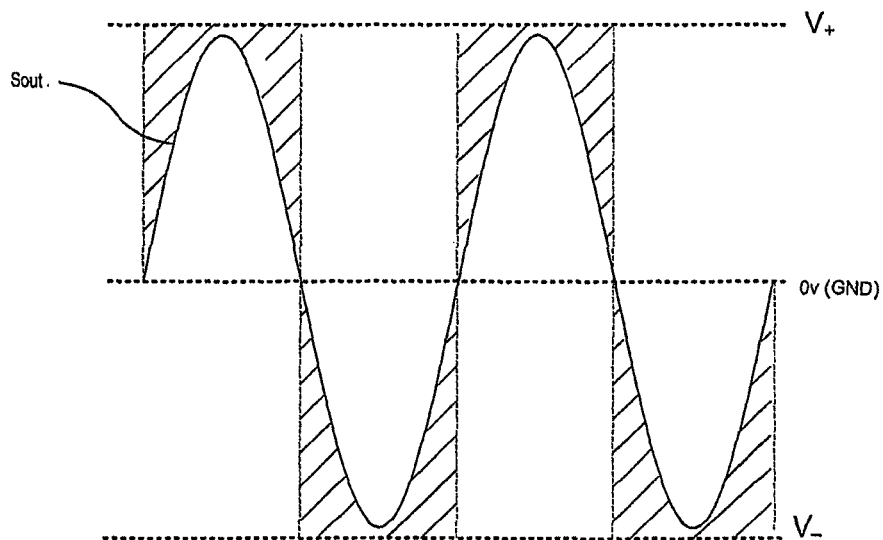
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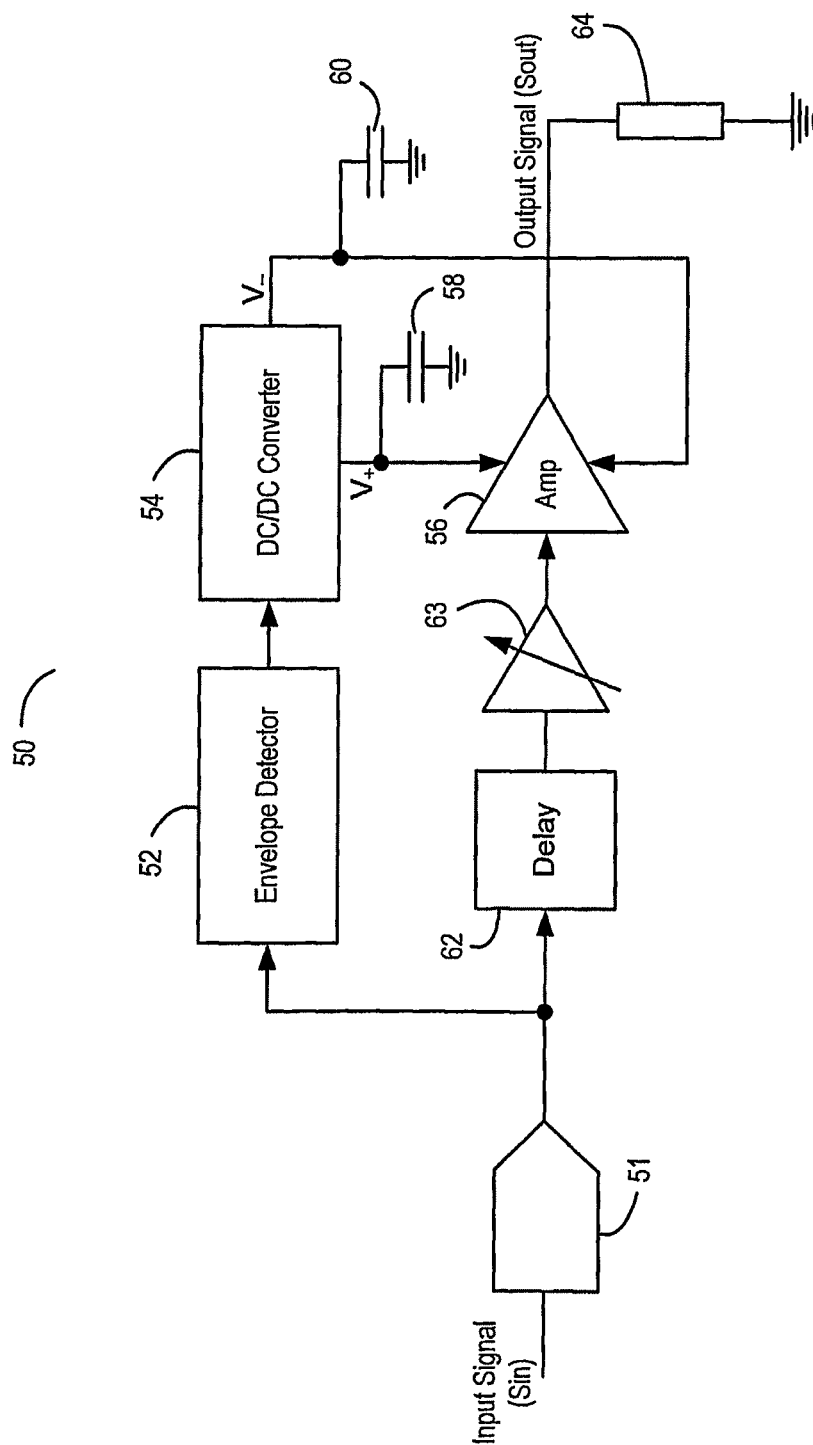
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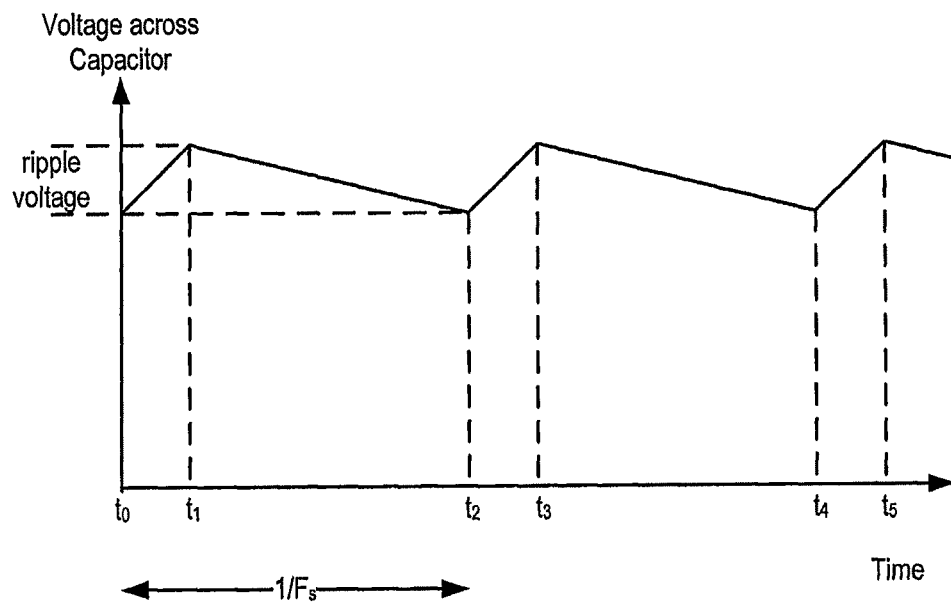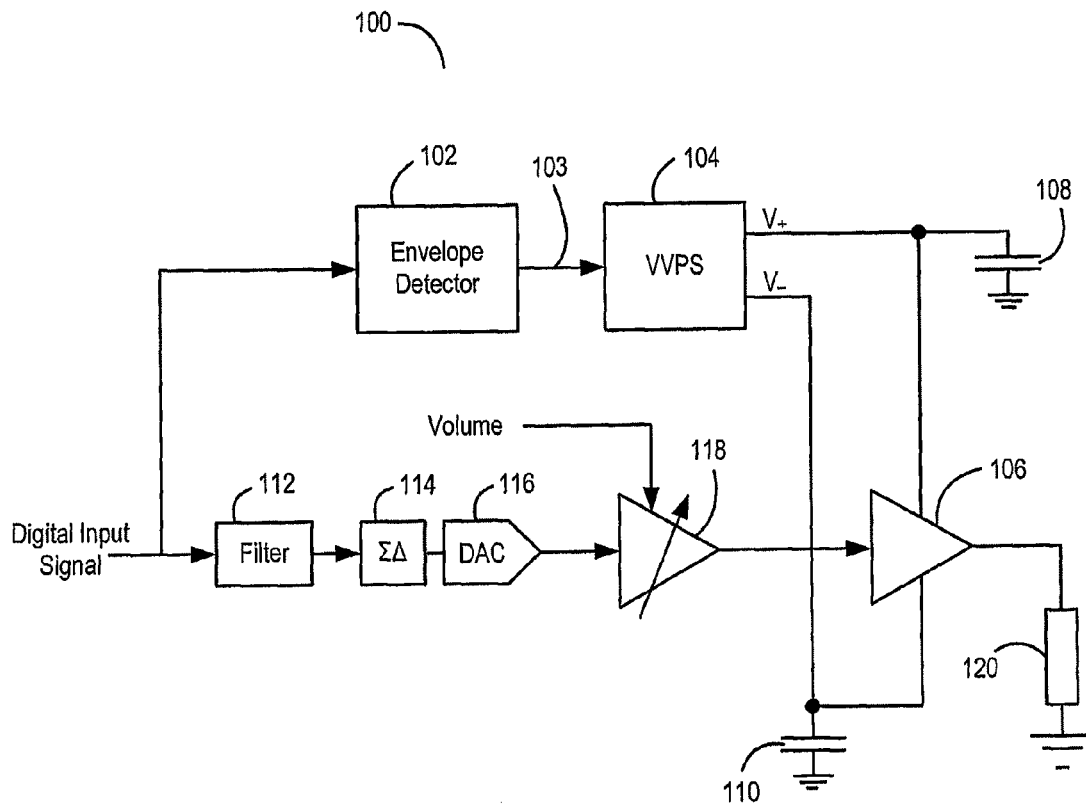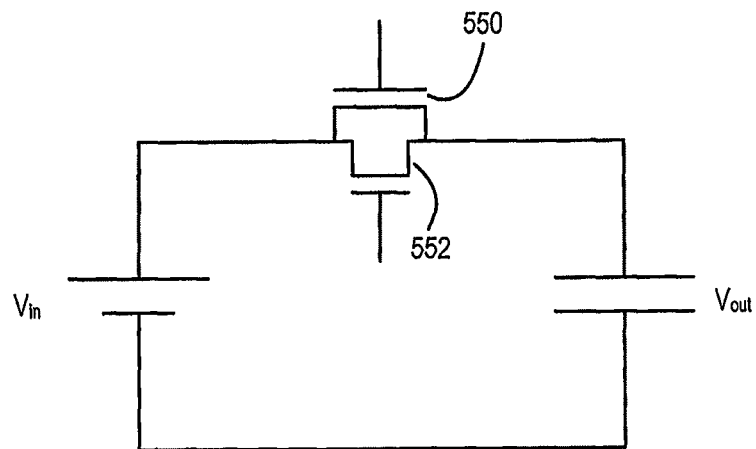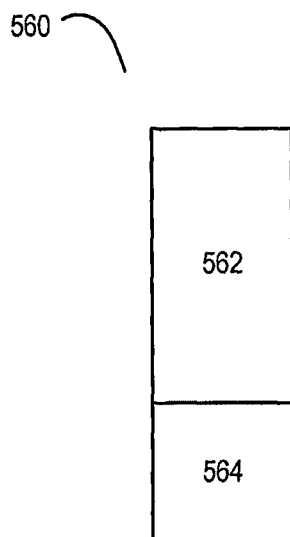
Figure 4

Figure 5

Figure 6
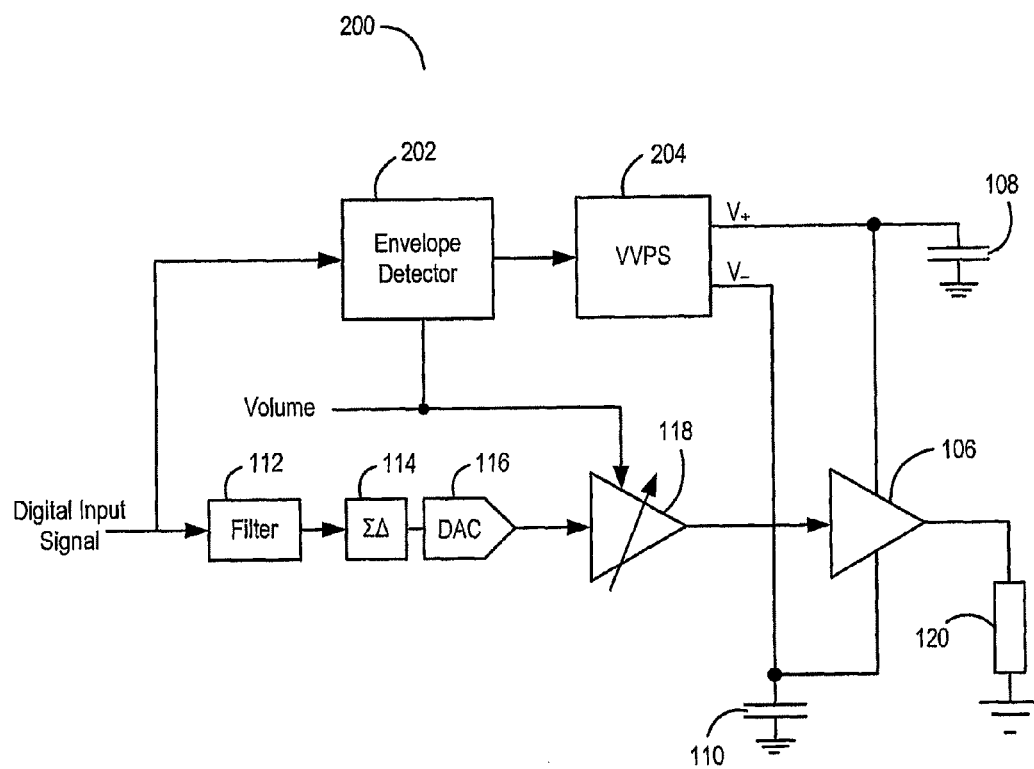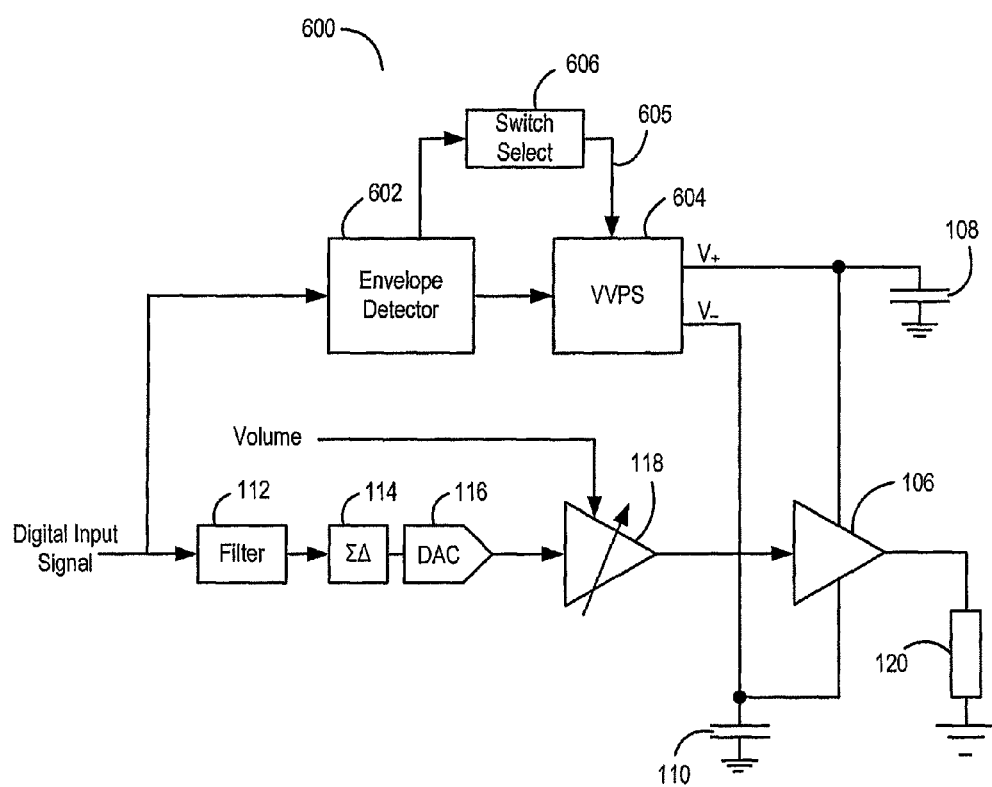
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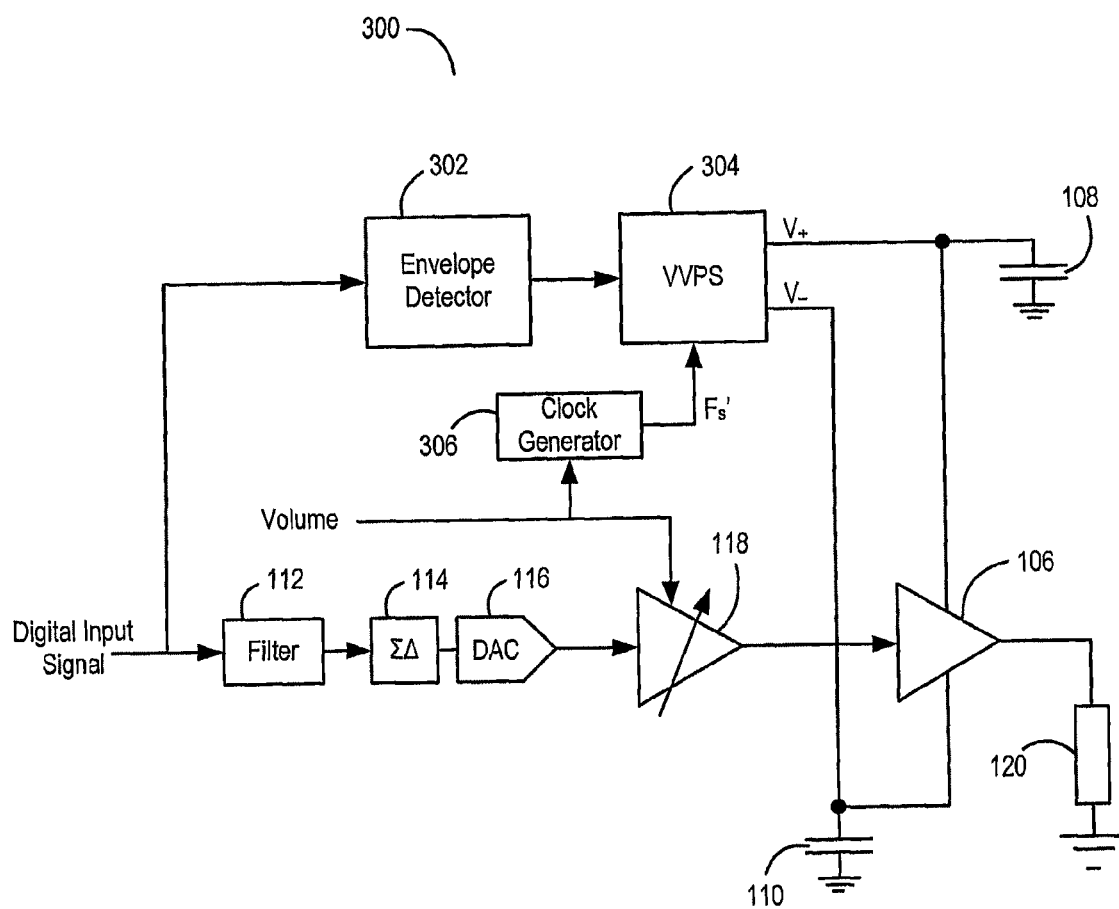
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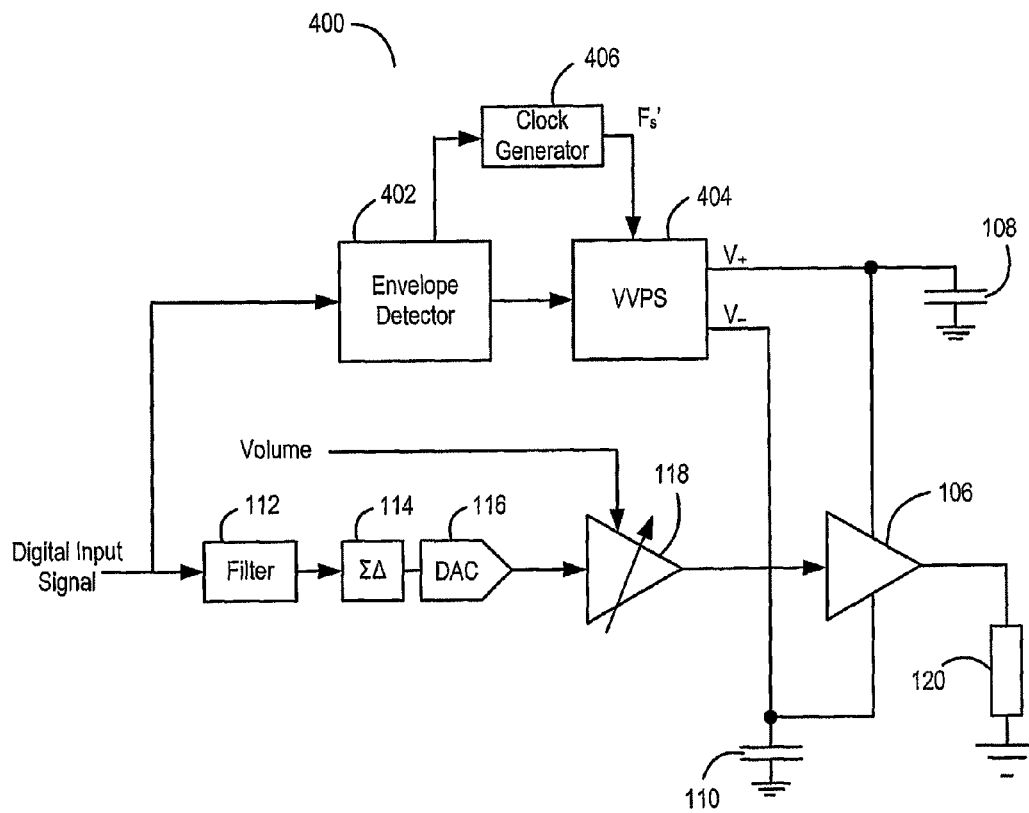
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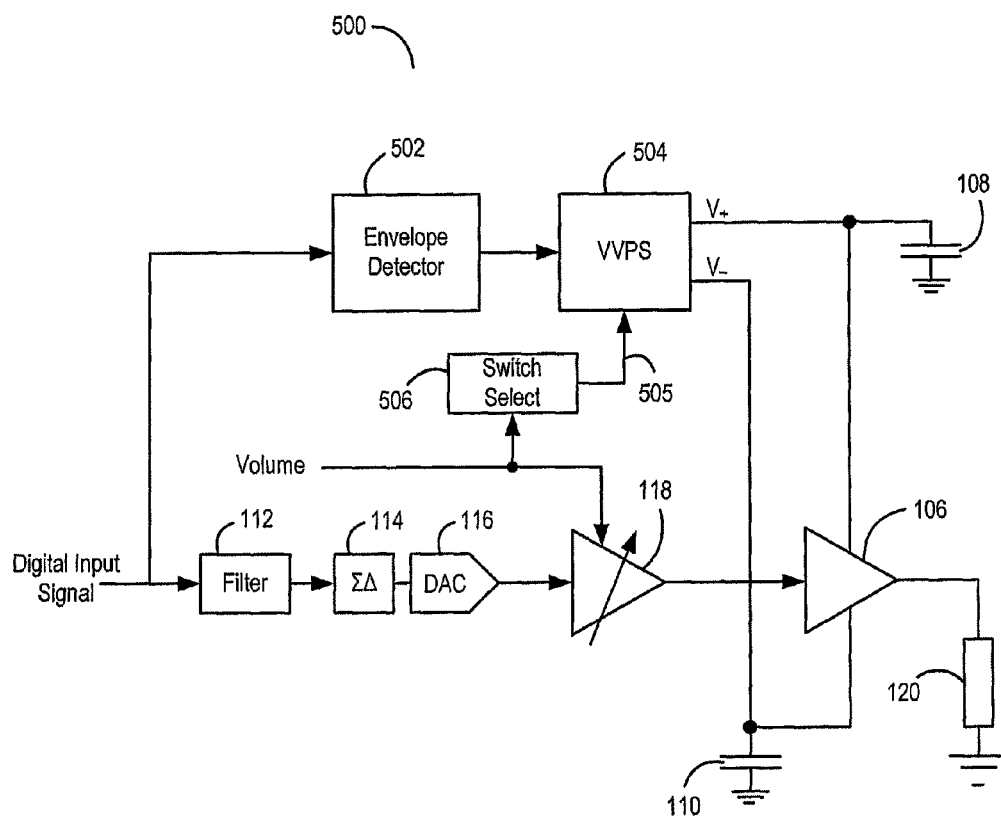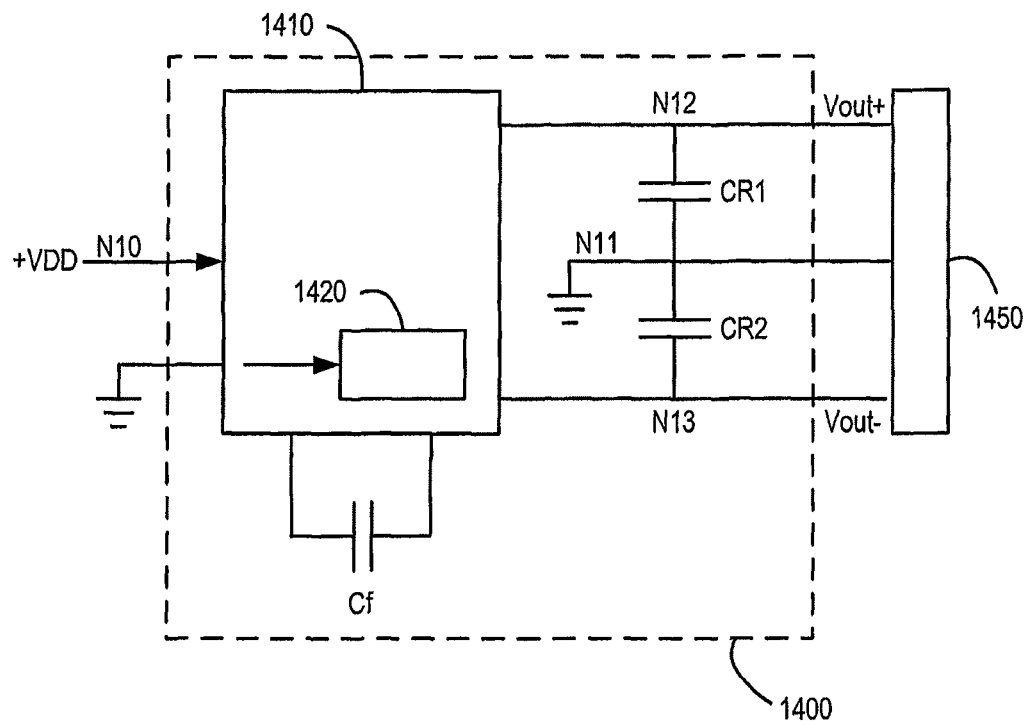
Figure 10

Figure 11

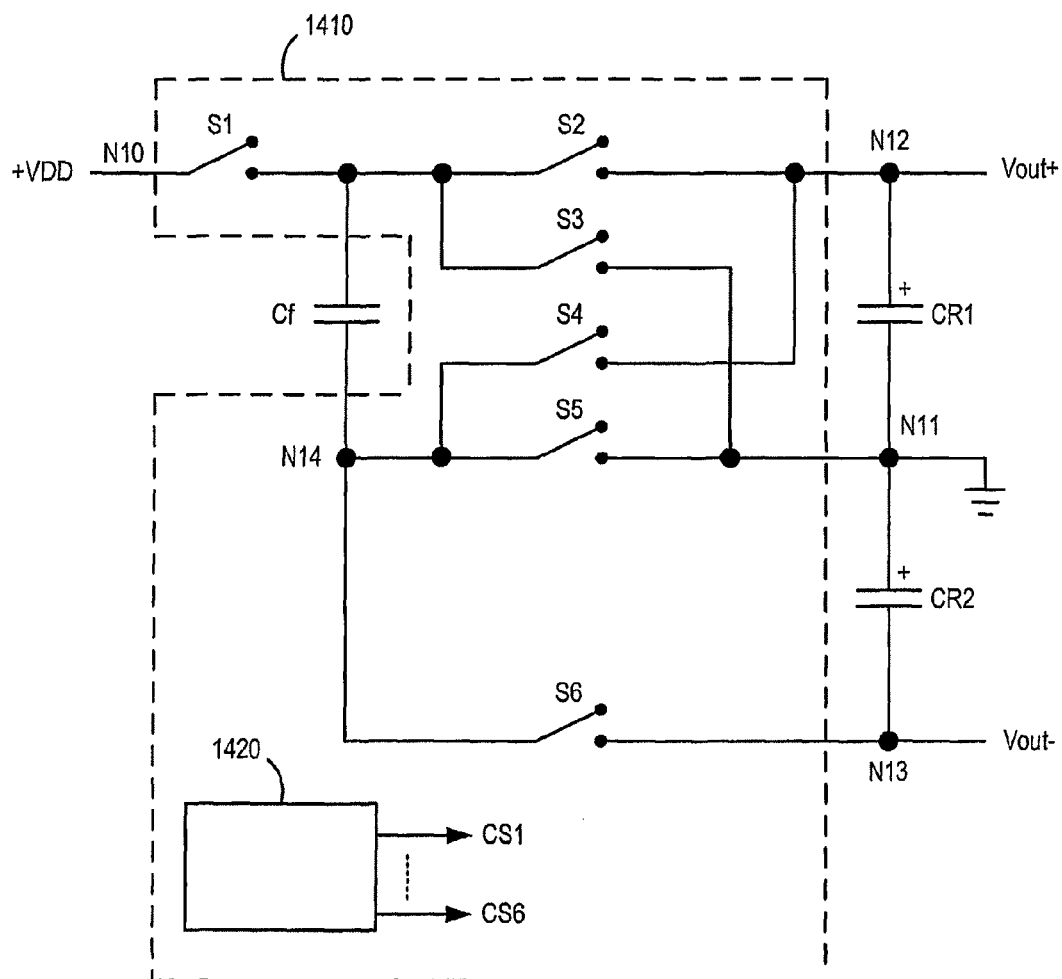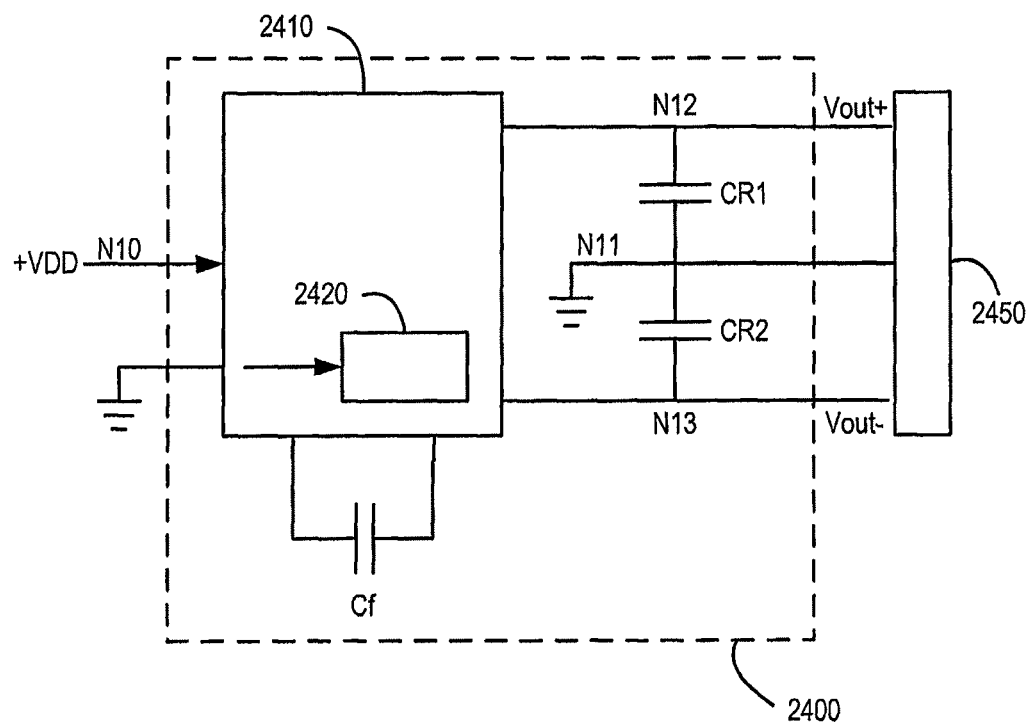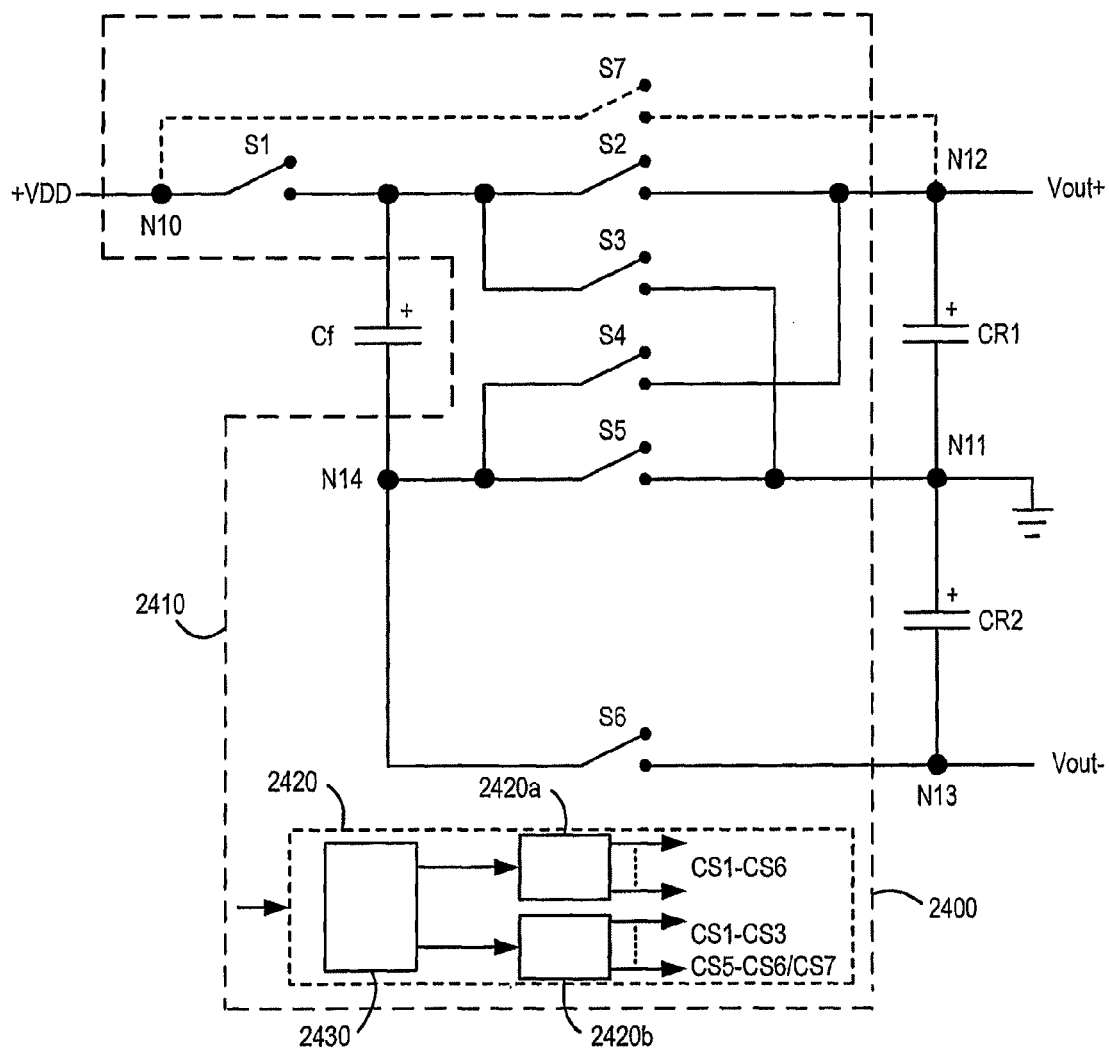Figure 12

Figure 13

Figure 14a

Figure 14b

Figure 15a

Figure 15b

AMPLIFIER CIRCUIT

This invention relates to amplifier circuits, and in particular but not exclusively to amplifier circuits that include power amplifiers.

BACKGROUND

FIG. 1 shows a basic Class AB amplifier 10. A bipolar (i.e. split level) power supply outputs the voltages V_+, V_- and these output voltages are applied across the amplifier 10, which amplifies the input signal S_{in} and outputs a ground-referenced amplified output signal S_{out} to a load 20. Provided the voltages supplied to the amplifier 10 are sufficient, the amplifier 10 has a substantially linear amplification (ignoring crossover effects). That is, the voltages V_+, V_- output from the power supply must be adequate so as to avoid output signal "clipping", i.e. attenuation of the output when the signal nears, equals or exceeds the voltages V_+, V_- output from the power supply to the amplifier. This is avoided by having "headroom" between the maximum output signal S_{outmax} and the power supply rails.

FIG. 2 is a graph showing S_{out} where S_{in} is a sine wave.

In this example, V_+ and V_- are set sufficiently high so that the input sine wave is linearly amplified. That is, there is a small amount of headroom between V_+ and V_- and the maximum output signal, so that the signal is not clipped.

The shaded region of the graph is representative of the power wasted in the amplifier 10; it can be seen that the amplifier 10 is very efficient when the output is close to V_+ or but very inefficient when the output is close to 0 V (GND). That is, a large amount of power is still being expended by the amplifier 10 even when the output signal S_{out} is small. The maximum theoretical efficiency for a class AB amplifier is 78.5%.

Class G amplifiers overcome this limitation on efficiency by providing more than one set of power supply rails, i.e. supply voltages. That is, as shown in FIG. 3, the amplifier may run off one power supply V_+-V_- if the output signal S_{out} is reasonably large, or another smaller power supply V_p-V_n if the output signal S_{out} is small. Ideally, an infinite number of power supply rails would be provided, such that the voltage supplied to the amplifier effectively "tracks" the input signal, always providing just enough voltage so that there is no clipping.

FIG. 4 shows an example of a Class G amplifier 50.

A digital signal S_{in} to be amplified is input to the amplifier 50. The digital input signal is first converted to an analogue signal by a digital-to-analogue converter (DAC) 51. The resulting analogue signal is fed to an envelope detector 52. The envelope detector 52 detects the size of the envelope of the analogue output signal of the DAC 51, and outputs a control signal to a switching DC-DC converter 54. The control signal is indicative of the size of the envelope of the analogue output of the DAC 51. The DC-DC converter 54 then supplies voltages V_+ and V_- to a power amplifier 56 by charging respective capacitors 58, 60. The voltages V_+ and V_- supplied by the DC-DC converter 54 vary with the control signal from the envelope detector 52, such that a relatively large envelope will lead to a relatively high voltage supplied to the power amplifier 56; conversely, a small envelope will lead to a relatively small voltage being supplied to the power amplifier 56, so that less power is wasted.

V_+ is supplied to one terminal of a first capacitor 58, and V_- is supplied to one terminal of a second capacitor 60. The second terminals of the respective capacitors 58, 60 are

connected to ground. The DC-DC converter 54 is switched on and off at a fixed frequency F_s, so that the capacitors 58, 60 are alternately charged and discharged, with an approximately constant voltage being applied to the power amplifier 56 provided the envelope of the analogue signal does not change.

FIG. 5 is a schematic graph illustrating the voltage across one of the capacitors 58, 60 (in practice the charge and discharge profiles of the capacitor will be exponential curves). At time t_0, the DC-DC converter 54 is switched on and the capacitor begins to charge. At time t_1, the DC-DC converter 54 is switched off and the capacitor begins to discharge. At time t_2, the DC-DC converter 54 is switched on and the capacitor begins to charge again. This action repeats, such that the voltage across the capacitor is maintained at an approximately constant level, with a small amount of variation known as the "ripple voltage". The time period between t_0 and t_2, therefore, is $1/F_s$.

In parallel with the envelope detection discussed above, the analogue output signal of the DAC 51 in FIG. 4 is fed through an analogue delay 62 to a preamplifier 63, typically a programmable gain amplifier (PGA), which amplifies the delayed signal by a gain set in accordance with a received control signal (i.e. the volume). The output from the preamplifier 63 is fed to the power amplifier 56, where it is amplified and output to a load 64. The analogue delay 62 is necessary so that the power modulation achieved by the envelope detection is synchronized with the signal arriving at the power amplifier 56.

However, analogue delays often cause distortion of the signal; the longer the delay that is required, the worse the distortion of the delayed signal. Conventionally, to minimize this effect, the envelope detection and power modulation must be made to operate as quickly as possible; that is, the DC-DC converter 54 must react quickly to changes in the input signal. However, this approach also has drawbacks. For example, where the power amplifier 56 is used to amplify an audio signal, a DC-DC converter that operates at the frequencies necessary to reduce distortion in the signal may itself generate noise tones that are audible to a user.

In practice, a compromise needs to be, reached between distortion of the signal and noise generated by the power supply.

SUMMARY OF INVENTION

According to one aspect of the present invention, there is provided an amplifier circuit comprising: an input, for receiving an input signal to be amplified; a preamplifier, for amplifying the input signal based on a variable gain; a power amplifier for amplifying the signal output from the preamplifier; a variable voltage power supply for supplying power to the power amplifier, said power being adjusted based on the variable gain.

According to a related aspect of the present invention, there is provided a method of amplifying a signal, comprising the steps of: receiving an input signal; amplifying the input signal in a preamplifier based on a variable gain; supplying power from a variable voltage power supply to a power amplifier; and amplifying the analogue signal in the power amplifier, wherein the variable voltage power supply is controlled based on the input signal and the variable gain.

According to another aspect of the present invention, there is provided an amplifier circuit, comprising: an input, for receiving an input digital signal to be amplified; a delay block for delaying the input digital signal and outputting an analogue signal, the delay block comprising a digital-to-

analogue converter for receiving the digital signal and converting the digital signal to an analogue signal; a power amplifier for amplifying the analogue signal; and a variable voltage power supply for supplying at least one supply voltage to the power amplifier, wherein the at least one supply voltage supplied by the variable voltage power supply is controlled based on the input digital signal.

According to a related aspect of the invention, there is provided a method of amplifying a signal. The method comprises the steps of: receiving an input digital signal; converting the delayed digital signal to analogue; supplying at least one supply voltage from a variable voltage power supply to a power amplifier; and amplifying the analogue signal in the power amplifier, wherein the at least one supply voltage supplied by the variable voltage power supply is controlled based on the input digital signal.

According to another aspect of the present invention, there is provided an amplifier circuit, comprising: an input, for receiving an input signal to be amplified; a preamplifier, for amplifying the input signal based on a volume signal; a power amplifier for amplifying the signal output from the preamplifier; a clock generator for generating a clock signal, the clock signal having a frequency that varies in accordance with the volume signal; and a switched power supply for receiving said clock signal, switching at said clock signal frequency, and supplying at least one supply voltage to the power amplifier.

According to a related aspect of the invention, there is provided a method of amplifying a signal. The method comprises the steps of receiving an input signal; amplifying the input signal in a preamplifier in accordance with a volume signal; supplying at least one supply voltage from a switched power, supply to a power amplifier; and amplifying the signal output from the preamplifier in the power amplifier, wherein the switched power supply is switched at a frequency that varies in accordance with the volume signal.

According to another aspect of the present invention, there is provided an amplifier circuit, comprising: an input, for receiving an input signal to be amplified; a power amplifier for amplifying the input signal; a clock generator for generating a clock signal, the clock signal having a frequency that varies with the input signal; and a switched power supply for receiving said clock signal, switching at said clock signal frequency, and supplying at least one supply voltage to the power amplifier.

According to a related aspect of the invention, there is provided a method of amplifying a signal. The method comprises the steps of: receiving an input signal; supplying at least one supply voltage from a switched power supply to a power amplifier; and amplifying the input signal in the power amplifier, wherein the switched power supply is switched at a frequency that varies in accordance with the input signal.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, and to show more clearly how it may be carried into effect, reference will now be made, by way of example, to the following drawings, in which:

FIG. 1 shows a basic class AB amplifier;

FIG. 2 shows an output signal from the amplifier of FIG. 1 when the input signal is a sine wave;

FIG. 3 illustrates dual supply rails used in an amplifier;

FIG. 4 shows a typical class G amplifier;

FIG. 5 is a schematic graph modelling the voltage across one of the capacitors in FIG. 4;

FIG. 6 shows an amplifier according to one aspect of the present invention;

FIG. 7 shows an amplifier according to another aspect of the present invention;

FIG. 8 shows an amplifier according to another aspect of the present invention;

FIG. 9 shows an amplifier according to another aspect of the present invention;

FIG. 10 shows another amplifier;

FIG. 11 shows an example of the switches that may be used in the amplifier of FIG. 10;

FIG. 12 shows an example implementation of the switches of FIGS. 10 and 11;

FIG. 13 shows a further amplifier;

FIGS. 14a and 14b show a first charge pump suitable for use with any of the amplifiers of the present invention; and

FIGS. 15a and 15b show a second charge pump suitable for use with any of the amplifiers of the present invention.

DETAILED DESCRIPTION

FIG. 6 shows an amplifier 100 for use in amplifying audio signals according to one aspect of the present invention. However, it will be appreciated that the amplifier 100 can be used for amplifying many other types of signal.

The amplifier 100 receives a digital input signal to be amplified. The digital input signal is input to an envelope detector 102. The envelope detector 102 detects the size of the envelope of the digital input signal and outputs a control signal 103 to a variable voltage power supply (VVPS) 104. The control signal 103 output to the VVPS 104 is indicative of the size of the detected envelope. The VVPS 104 in turn provides two voltages V^+ and V_- to a power amplifier 106 by charging respective capacitors 108, 110. As the control signal 103 from the envelope detector 102 varies, the voltages V_+ and V_- supplied by the VVPS 104 vary such that a control signal indicative of a relatively large envelope will lead to a relatively high voltage supplied to the power amplifier 106; conversely, a control signal indicative of a relatively small envelope will lead to a relatively small voltage being supplied to the power amplifier 106, so that less power is wasted.

V_+ is supplied to one terminal of a first capacitor 108, and V_- is supplied to one terminal of a second capacitor 110. The second terminals of the respective capacitors 108, 110 are connected to ground. The VVPS 104 is switched on and off at a frequency F_s, so that the capacitors 108, 110 are alternately charged and discharged, with an approximately constant voltage being supplied to the power amplifier 106 provided, the envelope of the digital input signal does not change.

The control signal 103 may have a high number of bits, for representing the size of the envelope with a high degree of accuracy. Alternatively, the control signal 103 may have only a single bit.

In parallel with the envelope detection, the digital input signal is input to a digital filter 112. The filtered signal is then input to a sigma-delta ($\Sigma\Delta$) modulator 114. The modulated filtered signal is input to a digital-to-analogue converter (DAC) 116, and converted to an analogue signal.

The effect of the filter 112, sigma-delta modulator 114 and DAC 116 is to convert the digital signal to an analogue signal so that it may be amplified, and to delay the signal so that its arrival at the power amplifier 106 is synchronized with the correct voltage levels as determined by the envelope detector 102. Thus in principle all that is required is a digital delay and a DAC. In the example shown in FIG. 6,

the delay is primarily introduced in the digital filter 112, although the sigma-delta modulator 114 and DAC 116 also have inherent delays. The sigma-delta modulator 114 reduces the word length of the input signal as will be familiar to those skilled in the art. This simplifies the DAC 116, as the input signal may be complex (audio signals typically have 24 bits), and designing a 24-bit DAC is very difficult. By reducing the word length using the sigma-delta modulator 114, or any other suitable word-length reduction block, the design of the DAC 116 is greatly simplified. The sigma-delta modulator 114 requires that the signal be upsampled, and this is the purpose of the digital filter 112.

The analogue output signal of the DAC 116 is input to a preamplifier 118 that amplifies the signal by a variable gain. The variable gain is set by a control signal, which in this particular example is the volume signal. In the majority of audio applications, the variable gain will typically be an attenuation, in order to improve the signal to noise ratio (SNR).

The preamplified signal is output from the preamplifier 118 to the power amplifier 106, where it is amplified and output to a load 120, such as, for example, a speaker, a set of headphones, or a line-out connector.

The amplifier 100 has a number of advantages over the amplifier 50 described with respect to FIG. 4. By detecting the envelope of the digital input signal, the amplifier 100 can make use of digital delays to delay the signal in parallel to the envelope detection. Digital delays are easy to implement and do not lead to distortion of the signal. Further, the digital delay can be easily adapted so the VVPS 104 need not operate as quickly as in the prior art, and so no tones are generated that may be audible to the user.

As described above, the digital delay can be realized using one or more processes that have an inherent delay. For example, the arrangement shown in FIG. 6 (i.e. the combination of the digital filter 112 and the sigma-delta modulator 114) simplifies the DAC 116 and also delays the signal; however, equalizer circuitry could be used to modulate and delay the signal; alternatively stereo or 3D processing would also delay the signal. This list is not exhaustive, however; any process or combination of processes that delays the signal could be used. It will also be appreciated that the delay could be provided by the DAC 116 alone.

The envelope detector 102 may take a number of forms that would be familiar to a person skilled in the art. For example, the envelope detector 102 may detect the envelope and compare it with some threshold value. In the case where the control signal 103 is only a single bit, the envelope detector 102 may comprise a comparator, that compares the envelope with a threshold value. If the envelope is below the threshold, the VVPS 104 will provide a relatively low voltage; if the envelope is above the threshold, the VVPS 104 will provide a relatively high voltage.

According to another example, the control signal 103 may be derived directly from the digital input signal, for example based on a certain bit, such as the most significant bit (MSB) of the input signal. According to this example, when the MSB is high the VVPS 104 will provide the higher supply voltage to the power amplifier 106; when the MSB is low the VVPS will provide the lower supply voltage to the power amplifier 106.

It will be appreciated that further bits of accuracy may be provided to the control signal 103, for example when using multiple power supply rails or voltage levels for powering the power amplifier 106, by using additional comparators and corresponding threshold values.

The variable voltage power supply 104 may take any one of a number of forms familiar to those skilled in the art. The VVPS 104 may be a charge pump, a DC-DC converter, or other switched-mode power supply. Further, although the VVPS 104 shown is a switched power supply, the amplifier 100 may use a non-switched power supply (e.g. a linear regulator). Also, the VVPS 104 shown in FIG. 6 provides a positive and a negative voltage output to the power amplifier; however, this is not necessary. The VVPS may supply only one voltage to the power amplifier. FIGS. 14 and 15, described below, illustrate two charge pumps that may be used as the VVPS 104.

FIG. 7 shows an amplifier 200 according to another aspect of the present invention.

The amplifier 200 is similar to the amplifier 100 described with respect to FIG. 6, with the exception of a number of components which will be described in more detail below. Components which are common to both amplifiers 100, 200 have retained their original reference numerals and will not be described further. The envelope detector 202 and VVPS 204 act in a similar way to their counterparts in the amplifier 100; however, the operation of either or both may be adjusted as described below.

In the amplifier 200, the control signal (i.e. volume signal) which is applied to the preamplifier 118 in order to set the variable gain in the preamplifier 118, is also used to adjust the voltages supplied to the power amplifier 106.

As described above, the variable gain applied in the preamplifier 118 is typically an attenuation in order to improve the signal-to-noise ratio. However, in the amplifier 100 the envelope detection, and therefore the voltages supplied to the power amplifier 106, is based on the full input signal. All of the gain in the system is present after the envelope detection. Thus, in the event that the volume results in an attenuation, there will be power wastage; if the volume results in a gain, there will be clipping of the signal output from the power amplifier 106.

There are a number of ways of achieving the application of volume to the envelope detection.

The input signal may be modified by the volume control signal before entering the envelope detector 202, such that the volume is already accounted for in the detected envelope (for example, the input signal may be multiplied by the volume signal).

Alternatively, the control signal output from the envelope detector 202 to the VVPS 204 may be modified by the volume, such that the VVPS 204 can adjust its voltage output accordingly (for example, the control signal may be multiplied by the volume). This latter method has the advantage of increasing the resolution of the system; the envelope detector 202 can use the full input signal to detect the envelope. Alternatively, the detecting mechanism of the envelope detector 202 may be adapted by the volume, in order to output a control signal that is adjusted for the volume. In a further alternative method, the output of the VVPS 204 may be adapted by the volume, so that the voltages supplied to the power amplifier 106 are adjusted for the volume.

The discussion above has described the application of the volume control signal not only to the pre-amplifier 118, as is conventional in order to set the variable gain within the pre-amplifier 118, but also to the envelope detection of the input signal. However, it will also be apparent to one skilled in the art that the variable gain itself may be applied to the envelope detection of the input signal. References above and below to adapting or modifying a quantity or signal "based on the volume" also therefore cover adapting that quantity or

signal based on the variable gain; the variable gain in the pre-amplifier by definition varies in accordance with the volume control signal, and thus varying or modifying a quantity or signal based on the variable gain is equivalent to indirectly varying or modifying that quantity or signal based on the volume.

The concept described above of applying volume to envelope detection in an amplifier, has so far been discussed only in relation to a digital input signal and a mixed-signal amplifier. However, it may easily be seen by one skilled in the art that application of volume gain to envelope detection will equally have benefits in a system with an analogue input signal and an analogue amplifier, as described with reference to FIG. **4**. For example, in the amplifier **50**, the volume may be applied either before, during or after the envelope detection in envelope detector **52**, as described earlier with reference to amplifier **200** and FIG. **7**.

FIG. **8** shows an amplifier **300** according to another aspect of the invention.

The amplifier **300** is similar to the amplifier **100** described with respect to FIG. **6**, with the exception of a number of components which will be described in more detail below. Components which are common to both amplifiers **100, 300** have retained their original reference numerals and will not be described further. The envelope detector **302** and VVPS **304** act in a similar way to their counterparts in the amplifier **100**; however, the operation of either or both may be adjusted as described below.

Similarly to the amplifiers described previously, the capacitors **108, 110** are charged when the VVPS **104** is switched on, and discharged when the VVPS **104** is switched off. As stated above, the magnitude of the rise and fall of the voltage across the capacitors **108, 110** is known as the "ripple voltage" (see FIG. **5**).

In order to reduce the ripple voltage across the capacitors **108, 110**, the switching frequency of the VVPS **304**, F_s, may be increased so that the capacitors **108, 110** do not discharge as much before being recharged. However, increasing the switching frequency F_s will result in greater power consumption within the VVPS **304** itself, as it will be switched on a greater number of times in a given period.

The rate of discharge of the capacitors **108, 110** is dependent on the amount of power that is dissipated in the load **120**, which is in turn dependent on the signal amplified by the power amplifier **106**. Before the signal reaches the power amplifier **106**, its envelope is detected and a variable gain (as set by the volume control signal) is applied to the input signal of the pre-amplifier **118**. Both of these factors (i.e. the signal envelope and the volume) have an effect on the signal that is input to the power amplifier **106**.

The amplifier **300** comprises a clock generator **306**, that receives the volume control signal and generates a clock signal with a frequency F_s'. The frequency F_s' of the clock signal is adapted to be relatively high when the volume is relatively high, and relatively low when the volume is relatively low. The clock signal is output to the VVPS **304**, such that the VVPS **304** switches at the frequency F_s'. Therefore, at higher volumes, where the current drawn in the load **120** is high, and thus the capacitors **108, 110** discharge relatively rapidly, the switching frequency F_s' of the VVPS **304** is also high. This means the voltage across the capacitors **108, 110** is maintained at an adequate level.

Conversely, if the volume is relatively low, less current will be drawn in the load **120**, and therefore the voltage across the capacitors **108, 110** will discharge relatively slowly. In this instance, the switching frequency F_s' may be lower, as the capacitors **108, 110** will not need to be charged

as frequently, and therefore power is saved. Although the embodiment of FIG. **8** is described as having first and second switching frequencies, it will be appreciated that multiple switching frequencies may be adopted.

FIG. **9** shows an amplifier **400** according to another aspect of the invention.

The amplifier **400** is similar to the amplifier **100** described with respect to FIG. **6**, with the exception of a number of components which will be described in more detail below. Components which are common to both amplifiers **100, 400** have retained their original reference numerals and will not be described further. The envelope detector **402** and VVPS **404** act in a similar way to their counterparts in the amplifier **100**; however, the operation of either or both may be adjusted as described below.

As described above, for a given load **120**, the amount of current drawn in the load **120** depends on the size of the envelope of the input signal. In view of this, the amplifier **400** comprises a clock generator **406** that receives a further control signal from the envelope detector **402**. The clock generator **406** generates a clock signal with a frequency F_s'. The clock signal is output to the VVPS **404**, such that the VVPS **404** switches at the frequency F_s'. Therefore, when the signal envelope is large, the current drawn in the load **120** will be high, and thus the capacitors **108, 110** will discharge relatively rapidly. Therefore, the switching frequency F_s' of the VVPS **404** is also high, such that the voltage across the capacitors **108, 110** is maintained at an adequate level.

Conversely, if the signal envelope is relatively low, less current will be drawn in the load **120**, and therefore the voltage across the capacitors **108, 110** will discharge relatively slowly. In this instance, the switching frequency F_s' may be lower, as the capacitors **108, 110** will not need to be charged as frequently, and therefore power is saved. Although the embodiment of FIG. **9** is described as having first and second switching frequencies, it will be appreciated that multiple switching frequencies may be adopted.

Both amplifiers **300, 400** may be adapted so that the switching frequency of the VVPS **304, 404** takes into account both the signal envelope and the volume. This may be achieved in a number of ways. For example, the volume may be applied to the envelope detector **302, 402** as described with reference to FIG. **7**. That is, in amplifier **400** the signal may be modified by the volume before the envelope is detected in the envelope detector **402** (for example, the signal may be multiplied by the volume); or the control signal output from the envelope detector **402** to the clock generator **406** may be modified by the volume (for example, the control signal may be multiplied by the volume). In amplifier **300**, the envelope detector **302** may output a control signal to the clock generator **306** such that both the envelope and the volume are taken into account when generating the clock signal. The person skilled in the art will be able to think of a multitude of ways in which the volume, the envelope, and their combination may be used to alter the switching frequency of the VVPS.

Further, it may easily be seen by one skilled in the art that application of volume, signal envelope, or their combination to the switching frequency will equally have benefits in a system with an analogue input signal and an analogue amplifier. Thus, an analogue amplifier, for example as described with reference to FIG. **4**, would comprise a clock generator as described with reference to FIGS. **8** and **9**, and operate in essentially the same way.

Two sources of power losses in switching power supplies are conduction losses and switching losses. Conduction

losses relate to the power dissipated by each switch of the switching power supply, and switching losses relate to the power dissipated in switching, i.e. driving, each switch. Typically switching power supplies use MOSFETs as the switching elements. A large MOSFET has a lower channel resistance, i.e. drain-source resistance R_{DS}, than a relatively smaller MOSFET for a given current. However, because of its relatively larger gate area, a large MOSFET will require a higher gate charge which results in greater switch driver current losses, i.e. switching losses, than smaller MOSFETs, for a given frequency of operation. While switching losses are typically less significant than conductive losses at high output currents, switching losses lead to significant inefficiencies at low output currents.

Thus, each time the VVPS is switched, the internal switches of the charge pump, for example, typically used to adjust the output voltage of the charge pump, expend some energy. This switching-loss energy is equal to $\frac{1}{2}CV^2$, where C is the capacitance of the switch, and V the voltage across the switch. Thus, in addition to being switched on a higher percentage of the time, the mere act of switching expends energy.

As mentioned above, the MOSFET switches in the VVPS have an inherent gate capacitance and an inherent channel resistance R_{DS}. Resistance R_{DS} is proportional to L/W, where L is the channel length of the MOSFET switch and W its channel width. The gate capacitance is proportional to the product WL.

$R \propto L/W$

$C \propto WL$

Therefore, increasing the width of a MOSFET switch increases its gate capacitance, and decreases its resistance. Decreasing the width has the opposite effect.

Many different types of switch may be used in the VVPS, e.g. single MOSFETs, transmission gates (i.e. NMOS and PMOS transistors), etc. However, the basic principle stated above is the same for each MOS switch type. The energy expended in operating the MOS switch is $\frac{1}{2}CV^2$, and the capacitance is proportional to the gate area (WL) of the switch.

FIG. 10 shows a further amplifier 500.

The amplifier 500 is similar to the amplifier 100 described with respect to FIG. 6, with the exception of a number of components which will be described in more detail below. Components which are common to both amplifiers 100, 500 have retained their original reference numerals and will not be described further. The envelope detector 502 and VVPS 504 act in a similar way to their counterparts in the amplifier 100; however, the operation of either or both may be adjusted as described below.

The amplifier 500 further comprises a switch select block 506 that receives the volume control signal and outputs a control signal 505 to the VVPS 504. The control signal 505 directs the VVPS 504 to adapt its switches as will be described in more detail below with reference to FIGS. 11 and 12.

FIG. 11 shows one example of the switches that may be used in VVPS 504. Two switches 550, 552 are connected in parallel between an input voltage V_{in} and an output voltage V_{out}. The first switch 550 is comparatively wide, and therefore has a comparatively low resistance and a high capacitance. The second switch 552 is narrower, and so has a higher resistance but a lower capacitance. In order to output a high voltage, low resistance is required in the switches of the VVPS 504 (i.e. in order to transfer as much as possible of V_{in} across to V_{out}). Therefore the wide switch 550 is used

in this instance. A greater amount of energy is expended as capacitance C is high, but this is necessary in order to achieve an adequate V_{out}.

However, if only a low output voltage is required, the resistance in the switches may be higher. Therefore, in this instance the narrower switch 552 could be used. The capacitance of the narrower switch 552 is lower, so less energy is spent in operating it. Although FIG. 11 shows just two switches, 550, 552 it will be appreciated that multiple switches, each having a different "width", may also be used.

FIG. 12 shows one possible implementation of the switches 550 and 552. A single switch 560 may be split unevenly as shown, into regions 562 and 564. This arrangement gives three possible switch widths: the smallest region 564; the larger region 562; and a region combining both 562 and 564. Alternatively, multiple switches may be provided, and different numbers of switches turned on in order to adapt the overall resistance and capacitance to desired values.

It can now be seen how the switch select block 506 in the amplifier 500 operates to reduce the power consumption of the amplifier 500. If the volume is high, a greater amount of voltage will be required in the capacitors 108, 110. Therefore, in this instance, the switch select block 506 directs the VVPS 504 to use relatively wide switches. If the volume is low, less voltage is required in the capacitors 108, 110. In this instance, the switch select block 506 directs the VVPS 504 to use relatively narrow switches, such that the switching losses in the VVPS 504 are minimized.

FIG. 13 shows a further amplifier 600.

The amplifier 600 is similar to the amplifier 100 described with respect to FIG. 6, with the exception of a number of components which will be described in more detail below. Components which are common to both amplifiers 100, 600 have retained their original reference numerals and will not be described further. The envelope detector 602 and VVPS 604 act in a similar way to their counterparts in the amplifier 100; however, the operation of either or both may be adjusted as described below.

The amplifier 600 further comprises a switch select block 606 that receives a control signal from the envelope detector 602 and outputs a control signal 605 to the VVPS 604. In an alternative arrangement, the switch select block 606 may receive the same control signal as is output to the VVPS 604. The control signal 605 directs the VVPS 604 to adapt its switches as described previously with reference to FIGS. 11 and 12.

If the signal envelope is relatively high, a greater amount of voltage will be required in the capacitors 108, 110. Therefore, in this instance, the switch select block 606 directs the VVPS 604 to use relatively wide switches. If the signal envelope is low, less voltage is required in the capacitors 108, 110. In this instance, the switch select block 606 directs the VVPS 604 to use relatively narrow switches, such that the switching losses in the VVPS 604 are minimized. As above, it will be appreciated that multiple switches may be used, each having a different "width".

Both amplifiers 500, 600 may be adapted so that the switch select block 506, 606 takes into account both the signal envelope and the volume. This may be achieved in a number of ways. For example, the volume may be applied to the envelope detector 502, 602 as described with reference to FIG. 7. That is, in the amplifier 600 the input signal may be modified by the volume before it is detected in the envelope detector 602 (for example, the signal may be multiplied by the volume); or the control signal output from the envelope detector 602 to the switch select block 606 may be modified by the volume (for example, the control signal

may be multiplied by the volume); or the control signal **605** output from the switch select block **606** may be modified by the volume signal. In the amplifier **500**, the envelope detector **502** may output a further control signal, indicative of the detected input signal envelope, to the switch select block **506** such that both the envelope and the volume are taken into account when generating the switch select control signal. The person skilled in the art will be able to think of a multitude of ways in which the volume, the envelope, and their combination may be used to alter the switches used in the VVPS.

Further, it may easily be seen by one skilled in the art that application of volume, signal envelope, or their combination to a switch select block will equally have benefits in a system with an analogue input signal and an analogue amplifier. Thus, an analogue amplifier, for example as described with reference to FIG. **4**, would comprise a switch select block as described with reference to FIGS. **10** and **13**, and operate in essentially the same way.

FIG. **14***a* shows a charge pump **1400** that is suitable for use as the VVPS **104**, **204**, **304**, **404**, **504**, **606** in any of FIGS. **6**, **7**, **8**, **9**, **10** and **13** respectively. Further, the charge pump **1400** is also suitable for use as the VVPS in any of the analogue equivalents of the amplifiers **200**, **300**, **400**, **500**, **600**.

FIG. **14***a* is a block diagram of a novel inverting charge pump circuit, which we shall call a "Level Shifting Charge-Pump" (LSCP) **1400**. There are two reservoir capacitors CR1 and CR2, a flying capacitor Cf and a switch array **1410** controlled by a switch controller **1420**. However, in this arrangement, neither of the reservoir capacitors CR1, CR2 are connected directly to the input supply voltage VDD, but only via the switch array **1410**. It should be noted that LSCP **1400** is configured as an open-loop charge-pump, although a closed-loop arrangement would be readily appreciated and understood by those skilled in the art. Therefore, LSCP **1400** relies on the respective loads (not illustrated) connected across each output N12-N11, N13-N11 remaining within predetermined constraints. The LSCP **1400** outputs two voltages Vout+, Vout– that are referenced to a common voltage supply (node N11), i.e. ground. Connected to the outputs Vout+, Vout–, N11, and shown for illustration only, is a load **1450**. In reality this load **1450** may be wholly or partly located on the same chip as the power supply, or alternatively it may be located off-chip. The load **1450** is a combination of the power amplifier **106** and the load **120**.

LSCP **1400** operates such that, for an input voltage +VDD, the LSCP **1400** generates outputs of magnitude +VDD/2 and –VDD/2 although when lightly loaded, these levels will, in reality, be +/–VDD/2—Iload.Rload, where (load equals the load current and Rload equals the load resistance. It should be noted that the magnitude (VDD) of output voltage across nodes N12 & N13 is the same, or is substantially the same, as that of the input voltage (VDD) across nodes N10 & N11.

FIG. **14***b* shows a more detailed version of the LSCP **1400** and, in particular, detail of the switch array **1410** is shown. The switch array **1410** comprises six switches S1-S6 each controlled by corresponding control signal CS1-CS6 from the switch controller **1420**. The switches are arranged such that first switch S1 is connected between the positive plate of the flying capacitor Cf and the input voltage source, the second switch S2 between the positive plate of the flying capacitor and first output node N12, the third switch S3 between the positive plate of the flying capacitor and common terminal N11, the fourth switch S4 between the negative plate of the flying capacitor and first output node N12,

the fifth switch S5 between the negative plate of the flying capacitor and common terminal N11 and the sixth switch S6 between the negative plate of the flying capacitor and second output terminal N13. It should be noted that the switches can be implemented in a number of different ways (for example, MOS transistor switches or MOS transmission gate switches) depending upon, for example, an integrated circuits process technology or the input and output voltage requirements.

FIG. **15***a* shows a further charge pump **2400** that is suitable for use as the VVPS **104**, **204**, **304**, **404**, **504**, **606** in any of FIGS. **6**, **7**, **8**, **9**, **10** and **13** respectively. Further, the charge pump **2400** is also suitable for use as the VVPS in any of the analogue equivalents of the amplifiers **200**, **300**, **400**, **500**, **600**.

FIG. **15***a* is a block diagram of a novel inverting charge pump circuit, which we shall call a "Dual Mode Charge Pump" (DMCP) **2400**. Again there are two reservoir capacitors CR1 and CR2, a flying capacitor Cf and a switch array **2410** controlled by a switch control module **420** (which may be software or hardware implemented). In this arrangement, neither of the reservoir capacitors CR1, CR2 are connected directly to the input supply voltage VDD, but rather via the switch array **2410**.

It should be noted that DMCP **2400** is configured as an open-loop charge-pump, although a closed-loop arrangement would be readily appreciated and understood by those skilled in the art. Therefore, DMCP **2400** relies on the respective loads (not illustrated) connected across each output N12-N11, N13-N11 remaining within predetermined constraints. The DMCP **2400** outputs two voltages Vout+, Vout– that are referenced to a common voltage supply (node N11). Connected to the outputs Vout+, Vout–, N11, and shown for illustration only, is a load **2450**. In reality this load **2450** may be wholly or partly located on the same chip as the power supply, or alternatively it may be located off-chip. The load **2450** is a combination of the power amplifier **106** and the load **120**.

DMCP **2400** is operable in two main modes. In a first mode the DMCP **400** operates such that, for an input voltage +VDD, the DMCP **2400** generates outputs each of a magnitude which is a mathematical fraction of the input voltage VDD. In the embodiment below the outputs generated in this first mode are of magnitude +VDD/2 and –VDD/2, although when lightly loaded, these levels will, in reality, be +/–VDD/2—Iload.Rload, where Iload equals the load current and Rload equals the load resistance. It should be noted that, in this case, the magnitude (VDD) of output voltage across nodes N12 & N13 is the same, or is substantially the same, as that of the input voltage (VDD) across nodes N10 & N11. In a second mode the DMCP **400** produces a dual rail output of +/–VDD.

FIG. **15***b* shows a more detailed version of the DMCP **2400** and, in particular, detail of the switch array **2410** is shown. The switch array **2410** comprises six main switches S1-S6 each controlled by corresponding control signal CS1-CS6 from the switch control module **2420**. The switches are arranged such that first switch S1 is connected between the positive plate of the flying capacitor Cf and the input voltage source, the second switch S2 between the positive plate of the flying capacitor and first output node N12, the third switch S3 between the positive plate of the flying capacitor and common terminal N11, the fourth switch S4 between the negative plate of the flying capacitor and first output node N12, the fifth switch S5 between the negative plate of the flying capacitor and common terminal N11 and the sixth switch S6 between the negative plate of the flying capacitor

and second output node N13. Optionally, there may be provided a seventh switch S7 (shown dotted), connected between the input voltage source (node N10) and first output node N12. Also shown in greater detail is the control module 2420 which comprises mode select circuit 2430 for deciding which controller 2420a, 2420b or control program to use, thus determining which mode the DMCP operates in. Alternatively, the mode select circuit 2430 and the controllers 2420a, 2420b can be implemented in a single circuit block (not illustrated).

In the first mode, switches S1-S6 are used and the DMCP 2400 operates in a similar manner to the LSCP 1400. In the second mode, switches S1-S3 and S5-S6/S7 are used, and switch S4 is redundant.

It should be noted that the switches can be implemented in a number of different ways (for example, MOS transistor switches or MOS transmission gate switches) depending upon, for example, an integrated circuit's process technology or the input and output voltage requirements.

The amplifiers described herein are preferably incorporated in an integrated circuit. For example, the integrated circuit may be part of an audio and/or video system, such as an MP3 player, a mobile phone, a camera or a satellite navigation system, and the system can be portable (such as a battery-powered handheld system) or can be mains-powered (such as a hi-fi system or a television receiver) or can be an in-car, in-train, or in-plane entertainment system. Further to the signals identified above, the signals amplified in the amplifier may represent ambient noise for use in a noise cancellation process.

The skilled person will recognise that some of the above-described apparatus and methods may be embodied as processor control code, for example on a carrier medium such as a disk, CD- or DVD-ROM, programmed memory such as read only memory (firmware), or on a data carrier such as an optical or electrical signal carrier. For many applications, embodiments of the invention will be implemented on a DSP (digital signal processor), ASIC (application specific integrated circuit) or FPGA (field programmable gate array). Thus the code may comprise conventional program code or microcode or, for example code for setting up or controlling an ASIC or FPGA. The code may also comprise code for dynamically configuring re-configurable apparatus such as re-programmable logic gate arrays. Similarly the code may comprise code for a hardware description language such as Verilog TM or VHDL (very high speed integrated circuit hardware description language). As the skilled person will appreciate, the code may be distributed between a plurality of coupled components in communication with one another. Where appropriate, the embodiments may also be implemented using code running on a field-(re-)programmable analogue array or similar device in order to configure analogue/digital hardware.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim, "a" or "an" does not exclude a plurality, and a single processor or other unit may fulfil the functions of several units recited in the claims. Any reference signs in the claims shall not be construed so as to limit their scope.

What is claimed is:

1. An amplifier circuit for amplifying an input signal and outputting an output signal, said input signal being amplified by a variable gain, said gain being controlled by a received volume signal, said circuit comprising;
  an amplifier for outputting said output signal; and
  a variable voltage power supply for supplying supply voltages to the amplifier, said supply voltages being variable based on a control signal,
  wherein the variable voltage power supply is a charge pump having flying capacitor terminals for connecting at least one flying capacitor and is operable, in use with just a single flying capacitor connected to said flying capacitor terminals, in first and second modes, wherein in the first mode the charge pump generates first positive and first negative supply voltages each substantially equal in magnitude to the magnitude of an input voltage and in the second mode the charge pump generates second positive and second negative output voltages each substantially equal in magnitude to half the magnitude of the input voltage, and wherein the charge pump selectively operates in said first mode or said second mode based on said control signal;
  wherein said control signal is based on at least one of the input signal and said received volume signal.

2. An amplifier circuit as claimed in claim 1, further comprising: an envelope detector for detecting the envelope of the input signal and outputting the control signal in accordance with the detected input signal envelope.

3. An amplifier circuit as claimed in claim 2, wherein the envelope detector is adapted to adjust said control signal based on the received volume signal.

4. An amplifier circuit as claimed in claim 2, wherein said control signal is adjusted based on the received volume signal after the control signal is output from the envelope detector.

5. An amplifier circuit as claimed in claim 1, wherein said flying capacitor terminals comprise first and second flying capacitor terminals and the charge pump comprises:
  an input terminal for receiving an input voltage;
  first and second output terminals; and
  a switch network for interconnecting said input terminal, said first and second flying capacitor terminals and said first and second output terminals, the switch network being operable to generate either said first positive and first negative supply voltages or said second positive and second negative supply voltages.

6. An amplifier circuit as claimed in claim 5 comprising a flying capacitor connected to said first and second flying capacitor terminals, a first reservoir capacitor connected to said first output terminal and a second reservoir capacitor connected to said second output terminal.

7. An amplifier circuit as claimed in claim 1 comprising:
  a delay block for receiving and delaying an input digital signal and outputting an analogue signal, the delay block comprising a digital-to-analogue converter for receiving the digital signal and converting the digital signal to an analogue signal.

8. An amplifier circuit as claimed in claim 7, further comprising:
  an envelope detector for detecting the envelope of the input digital signal and for outputting said control signal in accordance with the detected input digital signal envelope.

9. An amplifier circuit as claimed in claim 7, wherein the delay block comprises at least one of a filter, a sigma-delta modulator, and an equalizer block.

10. An amplifier circuit as claimed in claim 1 wherein said control signal takes one of two values.

11. An audio system, comprising an amplifier circuit as claimed in claim **1**.

12. An audio system as claimed in claim **11** wherein the audio apparatus comprises at least one: a portable music system, an MP3 player, a mobile telephone handset, a Hi-Fi, an in-car entertainment system and a DVD player.

13. A method of amplifying a signal, comprising:

receiving an input signal;

amplifying the input signal by a variable gain, said variable gain being controlled based on a received volume signal;

supplying positive and negative supply voltages from a variable voltage power supply to an amplifier; and

outputting an output signal from the amplifier,

wherein the positive and negative supply voltages supplied by the variable voltage power supply are generated by a charge pump having flying capacitor terminals for connecting at least one flying capacitor;

wherein said charge pump is operable, in use with just a single flying capacitor connected to said flying capacitor terminals, in first and second modes, wherein in the first mode the charge pump generates first positive and first negative supply voltages each substantially equal in magnitude to the magnitude of an input voltage and in the second mode the charge pump generates second positive and second negative output voltages each substantially equal in magnitude to half the magnitude of the input voltage;

wherein said charge pump is controlled to operate in said first or said second mode based on a control signal, wherein said control signal is based on at least one of the input signal and the received volume signal.

14. A method as claimed in claim **13**, further comprising:

detecting the envelope of the input signal; and

outputting the control signal in accordance with the detected input signal envelope.

15. A method as claimed in claim **14** wherein output of the envelope detection is adjusted by the received volume signal to provide said control signal.

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